MARKED UP VERSION OF REWRITTEN CLAIMS

34. (Amended) A chip scale package, provided by dividing a semiconductor wafer along scribe lines defining a plurality of chip scale package forming areas in said semiconductor wafer, comprising:

(a) a semiconductor chip having a main surface, a rear surface opposite to said main surface and a surface passivation film of a silicon nitride film to cover said main surface, said semiconductor chip having a plurality of semiconductor elements and bonding pads formed on said main surface thereof, said bonding pads being exposed from said surface passivation film;

(b) an elastomer layer of a polyimide film formed on said surface passivation film to cover said main surface of said semiconductor chip and to expose said bonding pads, said elastomer layer having an elastic modulus relatively lower than said surface passivation film;

(c) conductive layers formed on said elastomer layer, first ends of said conductive layers being disposed on said elastomer layer and second ends of said conductive layers being electrically connected to the corresponding ones of said bonding pads; and

(d) a plurality of bump electrodes formed on said elastomer layer, said plurality of bump electrodes being

electrically connected to said first ends of said conductive layers.